

What is claimed is:

1. An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data;

5 an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data;

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result; and

10 a limiter which outputs either said pulse code modulation data or a limit data in accordance with said detection result.

2. The apparatus for decoding encoded voice data according to claim 1, wherein said limit data has an upper limit data and a lower limit data; and wherein
15 said limiter comprises:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result;

a second comparator which compares said pulse code modulation data and said lower limit data and which outputs a second comparison result; and

20 a first output portion which outputs said pulse code modulation data, said

upper limit data or said lower limit data in accordance with said detection result and said first and second comparison results.

3. The apparatus for decoding encoded voice data according to claim 2,
5 wherein said first output portion comprises:

a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level;

a second logic circuit which outputs a second logic circuit result having said
10 first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level; and

a first selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, said lower limit data when said second logic circuit result having said first voltage level is input or said pulse code
15 modulation data when said first and second logic circuit results each not having said first voltage level is input.

4. The apparatus for decoding encoded voice data according to claim 1,
wherein a format of said limit data is the absolute value; and wherein said limiter
20 portion comprises:

a third comparator which compares a numerical value data of said pulse code modulation data and said limit data and which outputs a third comparison result; and

a second output portion which outputs said pulse code modulation data or
5 said limit data in accordance with said detection result and said third comparison result.

5. The apparatus for decoding encoded voice data according to claim 4, wherein said second output portion comprises:

10 a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level;

a second selector which selects said limit data when said third logic circuit result having said first voltage level is input or said numerical value data when said
15 third logic circuit result having said first voltage level is not input; and

a first combiner which combines a code data of said pulse code modulation data and said data selected by said second selector and which outputs a combined data.

20 6. The apparatus for decoding encoded voice data according to claim 4,

wherein said second output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level;

5 a second combiner which combines a code data of said pulse code modulation data and said limit data and which outputs a combined limit data; and

a third selector which selects said combined limit data when said third logic circuit result having said first voltage level is input or said pulse code modulation data when said third logic circuit result not having said first voltage level is input.

10 7. An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data;

15 an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data;

an error detector which detects whether an error is present in said encoded voice data and which outputs a detection result;

20 a first threshold value setting portion which calculates a limit data based on said pulse code modulation data and which outputs said limit data; and

wherein said apparatus further comprises:

a counter which counts the number of times that said pulse code modulation data is over said limit data and which outputs a count result having a first voltage level when said count result is over a predetermined value.

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11. The apparatus for decoding encoded voice data according to claim 10, wherein said limit data has an upper limit data and a lower limit data; and wherein said limiter comprises:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result;

a second comparator which compares said pulse code modulation data and said lower limit value and which outputs a second comparison result; and

a fourth output portion which does not outputs said pulse code modulation data when said count result is input having said first voltage level.

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12. The apparatus for decoding encoded voice data according to claim 11, wherein said fourth output portion comprises:

a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level;

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a second logic circuit which outputs a second logic circuit result having said first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level;

a first selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, said lower limit data when said second logic circuit result having said first voltage level is input or said pulse code modulation data when said first and second logic circuit results each not having said first voltage level is input; and

a controller which does not output said data output by said first selector when said count result is input having said first voltage level.

13. The apparatus for decoding encoded voice data according to claim 10, wherein a format of said limit data is the absolute value; and wherein said limiter portion comprises:

a third comparator which compares a numerical value data of said pulse code modulation data and said limit data and which outputs a third comparison result; and

a fifth output portion which does not outputs said pulse code modulation data or said limit data when said count result is input having said first voltage level.

14. The apparatus for decoding encoded voice data according to claim 13,
wherein said fifth output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first
voltage level when both a voltage level of said third comparison result and of said
5 detection result are said first voltage level;

a second selector which selects said limit data when said third logic circuit
result having said first voltage level is input or said numerical value data when said
third logic circuit result having said first voltage level is not input;

a first combiner which combines a code data of said pulse code modulation
10 data and said data selected by said second selector and which outputs a
combined data; and

a controller which does not output said combined data output by said first
combiner when said count result is input having said first voltage level.

15 15. The apparatus for decoding encoded voice data according to claim 13,
wherein said fifth output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first
voltage level when both a voltage level of said third comparison result and of said
detection result are said first voltage level;

20 a second combiner which combines a code data of said pulse code

modulation data and said limit data and which outputs a combined limit data; and

a third selector which does not select said combined limit data and said pulse code modulation when said count result is input having said first voltage level.

5 16. An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data;

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data;

10 an error detector which detects whether error is present in said encoded voice data and which outputs a detection result;

a second threshold value setting portion which calculates a limit data based on said pulse code modulation data produced at a term and which outputs said limit data, wherein said term is a term that a transmission error is not present in said encoded voice signal; and

15 a limiter which outputs either said pulse code modulation data or a limit data in accordance with said detection result.

20 17. The apparatus for decoding encoded voice data according to claim 16,

wherein said second threshold value setting portion comprises:

an average calculating portion which calculates an average value of a numerical value data of said pulse code modulation data and which outputs said average value; and

5 a third output portion which stores said average value based on the voltage levels of a control signal and said detection result and which outputs a stored average value.

18. The apparatus for decoding encoded voice data according to claim 17,
10 wherein said third output portion comprises:

a fourth logic circuit which outputs a fourth logic circuit result having said first voltage level when a voltage level of said control signal is said first voltage level and when a voltage level of said detection result is a second voltage level; and

a second latch portion which stores said average value based on a voltage
15 level of said fourth logic circuit result and which outputs a stored average value.